REMARKS

Claims 1-20 are in this application and are presented for consideration. By this Amendment, Applicant has amended claims 1, 12 and 17.

Claims 1-4, 12-15 and 17-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Myers et al. (US 5,400,950) in view of Gotman (US 4,404,453).

The present application names joint inventors. The Office Action states that in considering patentability of the claims under 35 U.S.C. 103(a), the Examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. To the best of Applicant's knowledge, the subject matter of the various claims was commonly owned at the time the invention was made.

The present invention relates to a process for producing a contact structure for connecting two substrates. The process comprises the step of applying solder material to terminal areas of a first substrate to form electrically active spacing metallizations with the solder material. The spacing metallizations are in direct contact with the terminal areas of the first substrate. The process further comprises the step of bonding the first substrate with a second substrate. The bonding between the terminal areas of the first substrate and a contact surface area of the second substrate is performed by means of a partial fusion of the spacing metallizations during the bonding action. The partial fusion of the spacing metallizations leaves an essential part of the spacing metallizations in a solidified state for providing space between the terminal areas and the contact surface area. The process advantageously allows good

electrical connection, a good mechanical connection and provides for necessary spacing with a simple and effective procedure.

These features and advantages are neither taught nor suggested by the prior art as a whole, including Myers et al. and Gotman. The references as a whole fail to teach and fail to suggest the combination of features as claimed. The prior art fails to suggest the novel combination of applying solder material to terminal areas of a first substrate to form electrically active spacing metallizations. This advantageously provides for an excellent mechanical connection having excellent conductivity.

Myers et al. is concerned with a method for controlling solder bump height for flip chip integrated circuit devices using a number of electrically inactive, dummy solder bumps. Myers et al. fails to teach or suggest the combination of an electrically active spacing between the terminal areas of the first substrate and a contact surface area of a second substrate. This electrically conductive spacer is significant in the present invention because it provides for a good electrical connection while achieving a spacing function between the first substrate and the second substrate. Myers et al. fails to teach or suggest that the dummy bumps 20 serve as an electrical connection. In fact, Myers et al. merely suggests that the dummy bumps 20 provide for only a spacing function. Myers et al. clearly discloses that the dummy bumps 20 are electrically inactive. (Column 5, lines 35-36). Myers et al. discloses solder bumps 16 are electrically active, however dummy bumps 20 are provided to support the height of the chip 12 since solder bumps 16 do not provide the necessary force to support the chip 12. As such, Myers et al. only suggests that the dummy bumps 20 serve as spacers and disadvantageously

fail to provide any electrical conductivity. In the present invention, the spacing metallizations advantageously provide both a mechanical and an electrical function so that separate solder bumps do not have to be used to mechanically and electrically connect the substrate as taught by Myers et al. The dummy bumps 20 disclosed in Myers et al. fail to provide one connection having such a duel function. The dummy bumps 20 of Myers et al. are exclusively used to provide a force against the chip 12 to obtain a certain height and are not electrically active as claimed. As such, the reference fails to teach and fails to suggest important aspects of the claimed combination.

Gotman takes a very different approach than Myers et al. Instead of being concerned with controlling solder bump height through a plurality of electrically inactive, dummy solder bumps, Gotman discloses heating a chip such that solder globules are liquified for contacting a contact pair (Column 3, lines 17-26, Column 4, lines 24-31). Gotman fails to teach and fails to suggest the electrical and mechanical connection and spacing as featured in the claimed combination. Gotman merely suggests bonding a chip 20 and a substrate 10 by backwards heating the chip 20 to fully melt solder globules 22 and 12 arranged on contact pairs 21 and 11. In the present invention, an essential part of the spacing metallizations are left in a solidified state to provide spacing as well as an electrical connection between the terminal areas and the contact surface area. This advantageously provides a secure mechanical connection having excellent electrical conductivity. Due to the complete reflow or melting of the globules 12 and 22 in Gotman, there cannot be any spacing action accomplished by the globules 22 and 12. In contrast to the present invention, Gotman teaches that the spacing function is achieved by

contact pairs 21 and 11. In the present invention, the spacing metallizations are partially melted to mechanically connect one substrate to another substrate. This advantageously provides a secure mechanical connection as well as an electrical connection that has good electrical conductivity. Gotman fails to provide such advantages since Gotman only teaches a spacing function that is created by contact pairs 21 and 11. As such, the reference fails to suggest important aspects of the claimed combination and fails to provide any teaching which would lead the person of ordinary skill in the art toward the combination claimed. Accordingly, Applicant respectfully requests that the Examiner favorably consider claims 1, 12 and 17 as now presented and all claims that respectively depend thereon.

Claims 5-9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Myers et al. in view of Leicht et al. (US 5,551,627). Although Leicht et al. teaches a solder connection structure that uses different types of materials that have different melting temperatures, the references as a whole fail to suggest the combination of features claimed. Specifically, Myers et al. fails to teach or suggest the combination of electrically conductive spacing metallizations between the terminal areas of the first substrate and the contact surface area of the second substrate. The references together do not teach or suggest the combination of features claimed. One of ordinary skill in the art is presented with various concepts, but these concepts do not provide any direction as to combining the features claimed. All claims define over the prior art as a whole.

Claims 10, 11 and 16 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Myers et al. and further in view of Beddingfield et al. (US 5,710,071). Although

Beddingfield et al. teaches a process for forming a flip-chip semi-conductor device by mounting a semiconductor die to a wiring substrate, the references as a whole fail to suggest the combination of features claimed. Specifically, Myers et al. fails to teach or suggest the combination of spacing metallizations that are left in a solidified state to provide spacing as well as an electrical connection between the terminal areas and the contact surface area as claimed. The references do not suggest the invention and therefore all claims define over the prior art as a whole.

Favorable consideration on the merits is requested.

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